WEST Search History

DATE: Thursday, September 02, 2004

Hide?	Set Name	Query	Hit Count
		DB=PGPB,USPT; THES=ASSIGNEE; PLUR=YES; OP=ADJ	
☐	L4	L3 and (plurality near states)	5
☐	L3	L2 and defect?	58
☐	L2	L1 and simulation	177
☐	L1	functional behavior and circuit and state?	322

END OF SEARCH HISTORY

IEEE HOME I SEARCH IEEE I SHOP I WEB ACCOUNT I CONTACT IEEE

◆IEEE

Membership Publications/Services Standards Conferences Careers/Jobs

IEEE Xplore®
RELEASE 1.8

Welcome
United States Patent and Trademark Office

» Sea

Help   FAQ   Terms   IEEE Peer Review   Quick Links

Welcome to IEEE Xplore®

○ Home
○ What Can I Access?
○ Log-out

Tables of Contents

○ Journals & Magazines
○ Conference Proceedings
○ Standards

Search

○ By Author
○ Basic
○ Advanced

Member Services

○ Join IEEE
○ Establish IEEE Web Account
○ Access the IEEE Member Digital Library

IEEE Enterprise

○ Access the IEEE Enterprise File Cabinet

Your search matched **1** of **1067317** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

Refine This Search:
You may refine your search by editing the current search expression or enteri
new one in the text box.

ho and functional behavior and circuit   Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine   **CNF** = Conference   **STD** = Standard
🔲 = Your access to full-text

---

1 **Efficient random vector verification method for an embedded 32-bit core**
*Chang-Ho Lee; Hoon-Mo Yang; Sung-Ho Kwak; Moon-Key Lee; Sanghyun Par
Sangyeun Cho; Sangwoo Kim; Yongchun Kim; Seh-Woong Jeong; Bong-Youn
Chung; Hyung-Lae Roh;*
ASICs, 2000. AP-ASIC 2000. Proceedings of the Second IEEE Asia Pacific
Conference on , 28-30 Aug. 2000
Pages:291 - 294

[Abstract]   [PDF Full-Text (396 KB)]   **IEEE CNF**

🖨 Print Format

Home | Log-out | Journals | Conference Proceedings | Standards | Search by Author | Basic Search | Advanced Search | Join IEEE | Web Account |
New this week | OPAC Linking Information | Your Feedback | Technical Support | Email Alerting | No Robots Please | Release Notes | IEEE Online
Publications | Help | FAQ| Terms | Back to Top

IEEE

Membership Publications/Services Standards Conferences Careers/Jobs

IEEE *Xplore*®
RELEASE 1.8

Welcome
United States Patent and Trademark Office

Help FAQ Terms IEEE Peer Review

Quick Links

» Sea

Welcome to IEEE *Xplore*®

- **Home**
- **What Can I Access?**
- **Log-out**

Tables of Contents

- **Journals & Magazines**
- **Conference Proceedings**
- **Standards**

Search

- **By Author**
- **Basic**
- **Advanced**

Member Services

- **Join IEEE**
- **Establish IEEE Web Account**
- **Access the IEEE Member Digital Library**

IEEE Enterprise

- **Access the IEEE Enterprise File Cabinet**

🖨 **Print Format**

Your search matched **3** of **1067317** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

Refine This Search:
You may refine your search by editing the current search expression or enteri new one in the text box.

| functional behavior and circuit and state? | **Search** |

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine   **CNF** = Conference   **STD** = Standard
🔲 = Your access to full-text

---

1 **An efficient modeling and synthesis procedure of asynchronous sequential logic circuits**
Kang, J.-W.; Wey, C.-L.; Fisher, P.D.;
Circuits and Systems, 1992., Proceedings of the 35th Midwest Symposium on 12 Aug. 1992
Pages:512 - 515 vol.1

[Abstract]   [PDF Full-Text (424 KB)]   **IEEE CNF**

---

2 **Behavioral testing of cellular neural networks**
Willis, J.; de Gyvez, J.P.;
Circuits and Systems, 1994. ISCAS '94., 1994 IEEE International Symposium on , Volume: 6 , 30 May-2 June 1994
Pages:229 - 232 vol.6

[Abstract]   [PDF Full-Text (388 KB)]   **IEEE CNF**

---

3 **Automating the design of asynchronous sequential logic circuits**
Wu, S.-F.; Fisher, P.D.;
Solid-State Circuits, IEEE Journal of , Volume: 26 , Issue: 3 , Mar 1991
Pages:364 - 370

[Abstract]   [PDF Full-Text (612 KB)]   **IEEE JNL**

Hit List

Search Results - Record(s) 1 through 5 of 5 returned.

☐ 1. Document ID: US 6539523 B1

Using default format because multiple data bases are involved.

L4: Entry 1 of 5   File: USPT   Mar 25, 2003

US-PAT-NO: 6539523
DOCUMENT-IDENTIFIER: US 6539523 B1

TITLE: Automatic formulation of design verification checks based upon a language representation of a hardware design to verify the intended behavior of the hardware design

DATE-ISSUED: March 25, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Narain; Prakash	San Carlos	CA		
Littlefield; Jay Andrew	San Jose	CA		
Morrison; Christopher Richard	Sunnyvale	CA		
Ranjan; Rajeev Kumar	Santa Clara	CA		

US-CL-CURRENT: 716/5; 716/4

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De |

☐ 2. Document ID: US 6493852 B1

L4: Entry 2 of 5   File: USPT   Dec 10, 2002

US-PAT-NO: 6493852
DOCUMENT-IDENTIFIER: US 6493852 B1

TITLE: Modeling and verifying the intended flow of logical signals in a hardware design

DATE-ISSUED: December 10, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Narain; Prakash	San Carlos	CA		
Kumar; Rajiv	Santa Clara	CA		

US-CL-CURRENT: 716/5; 716/4, 716/6

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De |

☐   3.   Document ID: US 6292765 B1

L4: Entry 3 of 5   File: USPT   Sep 18, 2001

US-PAT-NO: 6292765
DOCUMENT-IDENTIFIER: US 6292765 B1

TITLE: Method for automatically searching for functional defects in a description of a circuit

DATE-ISSUED: September 18, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Ho; Chian-Min Richard	Mountain View	CA		
Mardjuki; Robert Kristianto	Danville	CA		
Dill; David Lansing	Redwood City	CA		
Lin; Jing Chyuarn	Sunnyvale	CA		
Yeung; Ping Fai	San Jose	CA		
Estrada; Paul II	Los Alto	CA		
Giomi; Jean-Charles	Menlo Park	CA		
Ly; Tai An	Fremont	CA		
Mulam; Kalyana C.	San Jose	CA		
Widdoes, Jr.; Lawrence Curtis	San Jose	CA		
Wilcox; Paul Andrew	Palo Alto	CA		

US-CL-CURRENT: 703/14; 703/15, 703/16, 716/4

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De |

☐   4.   Document ID: US 6290539 B1

L4: Entry 4 of 5   File: USPT   Sep 18, 2001

US-PAT-NO: 6290539
DOCUMENT-IDENTIFIER: US 6290539 B1
** See image for Certificate of Correction **

TITLE: Electrical connector having a two-piece socket portion

DATE-ISSUED: September 18, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Wilber; Darrin F.	Metamora	MI		
Flowers; Robert J.	Ortonville	MI		

US-CL-CURRENT: 439/595

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De |

☐ 5.   Document ID: US 6012155 A

L4: Entry 5 of 5   File: USPT   Jan 4, 2000

US-PAT-NO: 6012155
DOCUMENT-IDENTIFIER: US 6012155 A

TITLE: Method and system for performing automatic extraction and compliance
checking of an IEEE 1149.1 standard design within a netlist

DATE-ISSUED: January 4, 2000

INVENTOR-INFORMATION:
NAME   CITY   STATE   ZIP CODE   COUNTRY
Beausang; James   Mountain View   CA
Singh; Harbinder   Cupertino   CA

US-CL-CURRENT: 714/727; 714/732

| Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D |

| Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS |

Term	Documents
PLURALITY	1928124
PLURALITIES	17227
PLURALITYS	2
STATES	488567
STATE	1376348
(3 AND (STATES NEAR PLURALITY)).PGPB,USPT.	5
(L3 AND (PLURALITY NEAR STATES)).PGPB,USPT.	5

Display Format: |- | | Change Format |

Previous Page   Next Page   Go to Doc#

Search for Application Number 08/954,765

First Search: Update Search: X

Date: 4/3/00

Background Info

Effective Filing Date
10/20/97

Inventor   Assignee
Ho et al.

Title
Method for Automated Search for Defects in a Description of a Circuit

Search

Classes/Subclasses

East Search

29	(RTL SAME (VERIF$ NEAR3 (DESIGN OR FUNCTIONS3)))	USPAT 2000/04/06 15:16
79	(RTL and (VERIF$ NEAR3 (DESIGN OR FUNCTION$3))) USPAT 2000/04/06 15:16	
72	(((RTL AND (VERIF$ NEAR3 (DESIGN OR FUNCTIONS3)))) AND SIMULAT$3) USPAT 2000/04/06 15:29	
2	(((((RTL AND (VERIF$ NEAR3 (DESIGN OR FUNCTION$3)))) AND SIMULAT$3)) AND (RESTOR$3 SAME STATE)) USPAT 2000/04/06 15:18	
7	(((((RTL AND (VERIF$ NEAR3 (DESIGN OR FUNCTION$3)))) AND SIMULAT$3)) AND (TEST ADJ PATTERN ADJ GENERAT$3)) USPAT 2000/04/06 15:37	
135	(Automat$5 adj TEST ADJ PATTERN ADJ GENERAT$3) USPAT 2000/04/06 15:38	
22	(((AUTOMAT$5 ADJ TEST ADJ PATTERN ADJ GENERAT$3)) AND ((NEXT ADJ STATE) OR (CURRENT ADJ STATE))) USPAT 2000/04/06 15:40	
40	(COVERAGE ADJ ANALYSIS) USPAT 2000/04/09 08:43	
5	(((COVERAGE ADJ ANALYSIS)) AND (SIMULAT$3 NEAR3 CIRCUIT)) USPAT 2000/04/09 08:43	

NPL Search

IEL – simulat* and function* and verif* and (restor* or reset*)
circuit and simulat* and verif* and (restor* or reset*)
circuit and simulat* and (restor* or reset*) and (current <word> state)
search <and> state <and> test <word> pattern
(test <word> pattern) and verif* and state

ACM – circuit verification
circuit verification simulation reset "current state" "future state" functional

GPI WEB CLIENT

Freeform Search

Database to Search:

```
US Patents
Japanese Patents
European Patents
USOCR Patents
```

Term: [   ]

Display [10] **Patents, Starting With #:** [1] **In Display Format:** [B]

Generate: ○ Hit List ◉ Hit Count ○ Image

[Search]   [Clear]

[Help]   [Comments]   [Logout]

[Main Menu]   [Show S Numbers]   [Edit S Numbers]

Search History

DB Name	Query	s	Set Name	Time
USPAT	#L8	0	L9	Wed Jul 14 12:30:35 1999
USPAT	17 and reset### and restor###		L8	Wed Jul 14 12:27:35 1999
USPAT	11 and (12 (p) 13)	2	L7	Wed Jul 14 12:27:09 1999
USPAT	#L5	1	L6	Wed Jul 14 12:26:09 1999
USPAT	11 and (12 (p) 13) and 14	1	L5	Wed Jul 14 12:22:47 1999
USPAT	restor### (p) reset###	1	L4	Wed Jul 14 12:22:17 1999
USPAT	vector# (3a) generat###	4	L3	Wed Jul 14 12:21:47 1999
USPAT	test### (w) vector#	23	L2	Wed Jul 14 12:20:41 1999
USPAT	(circuit# (3a) design###) (p) (test### or verif?)	77	L1	Wed Jul 14 12:19:42 1999

GPI WEB CLIENT

Freeform Search

Database to Search:

US Patents
Japanese Patents
European Patents
USOCR Patents

Term:

Display 10 **Patents, Starting With #:** 1 **In Display Format:** B

Generate: ○ Hit List ● Hit Count ○ Image

Search	Clear

Help	Comments	Logout

Main Menu	Show S Numbers	Edit S Numbers

Search History

DB Name	Query	Hits	Set Name	Time
USPAT	#L9	23	L10	Thu Jul 15 13:29:43 1999
USPAT	l8 and (test#== (w) vector#)	23	L9	Thu Jul 15 13:26:06 1999
USPAT	L1 and (count= or number#)	71	L8	Thu Jul 15 13:24:19 1999
USPAT	L1 and (test#== (w) vector#)	23	L7	Thu Jul 15 13:22:52 1999
USPAT	#L5	6	L6	Thu Jul 15 13:19:30 1999
USPAT	L1 (p) (test#== (w) vector#)	6	L5	Thu Jul 15 13:17:20 1999
USPAT	#L3	6	L4	Thu Jul 15 13:15:20 1999
USPAT	l1 and (test### (w) vector#)	6	L3	Thu Jul 15 13:14:37 1999
USPAT	l1 (p) (test### (w) vector#)	0	L2	Thu Jul 15 13:13:34 1999
USPAT	measur#### (p) ((fault# or test#) (3a) coverage#)	76	L1	Thu Jul 15 13:12:13 1999

GPI WEB CLIENT

Freeform Search

Database to Search:

- US Patents
- Japanese Patents
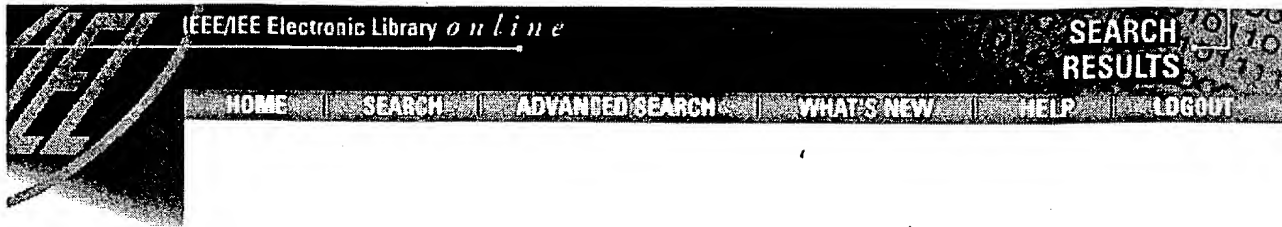- European Patents
- USOCR Patents

Term: [ ]

Display [10] **Patents, Starting With #:** [1] **In Display Format:** [B]

Generate: ○ Hit List ● Hit Count ○ Image

[Search] [Clear]

[Help] [Comments] [Logout]

[Main Menu] [Show S Numbers] [Edit S Numbers]

Search History

DB Name	Query	Hits	Set Name	Time
USPAT	#L8	20	L9	Thu Jul 15 15:27:38 1999
USPAT	l4 and l5	20	L8	Thu Jul 15 15:26:15 1999
USPAT	#L6	1	L7	Thu Jul 15 15:25:29 1999
USPAT	l4 (p) l5	1	L6	Thu Jul 15 15:23:55 1999
USPAT	circuit# (3a) (graph# or layout# or tree#)	6748	L5	Thu Jul 15 15:23:35 1999
USPAT	pattern# (3a) (identification or classification)	2083	L4	Thu Jul 15 15:20:33 1999
USPAT	#L2	16	L3	Thu Jul 15 15:14:09 1999
USPAT	l1 and (graph# (p) pattern#)	16	L2	Thu Jul 15 15:11:44 1999
USPAT	#S953	165	L1	Thu Jul 15 15:10:10 1999

IEEE/IEE Electronic Library *online*

HOME | SEARCH | ADVANCED SEARCH | WHAT'S NEW | HELP | LOGOUT

SEARCH RESULTS

((pattern <word> classification), <or> (pattern <wor | Refine

Collection: ☑ Journals ☑ Conferences ☑ Standards

Your search matched **27** of **545125** documents.

25 are presented on this page, sorted by Score in descending order.

DOC TYPE	VIEW ISSUE TOC	VIEW FULL PAGE	VIEW CITATION
CNF			**Input pattern classification for transistor level testing of bridging faults in BiCMOS circuits** *Menon, S.M.; Jayasumana, A.P.; Malaiya, Y.K.* VLSI, 1996. Proceedings., Sixth Great Lakes Symposium on , 1996 , Page(s): 214 -219
CNF			**Input pattern classification for detection of stuck-ON and bridging faults using I/sub DDQ/ testing in BiCMOS and CMOS circuits** *Menon, S.M.; Malaiya, Y.K.; Jayasumana, A.P.* VLSI Design. 1997. Proceedings., Tenth International Conference on , 1997 , Page(s): 545 -546
CNF			**Input pattern classification for transistor level testing of BiCMOS circuits** *Menon, S.M.; Jayasumana, A.P.; Malaiya, Y.K.* VLSI Test Symposium, 1994. Proceedings., 12th IEEE , 1994 , Page(s): 457 -462
PER			**A real-time clustering microchip neural engine** *Serrano-Gotarredona. T.; Linares-Barranco, B.* Very Large Scale Integration (VLSI) Systems, IEEE Transactions on Volume: 4 2 , June 1996 , Page(s): 195 -209
CNF			**A real time clustering CMOS neural engine** *Serrano-Gotarredona, T.; Linates-Barranco, B.; Huertas, J.L.* Circuits and Systems, 1995., Proceedings., Proceedings of the 38th Midwest Symposium on Volume: 2 , 1996 , Page(s): 978 vol.2
CNF			**Next Generation Test Generator (NGTG) for digital circuits** *Singer, S.; Vanetsky, L.* AUTOTESTCON, 97. 1997 IEEE Autotestcon Proceedings , 1997 , Page(s): 105 -112